REMARKS

Claims 1-23 are pending in the application. Claims 1-23 stand rejected under 35 U.S.C. 103(a) as allegedly being obvious in view of combinations of U.S. Patent No. 5,657,055 to Kansal et al. ("Kansal"), U.S. Patent No. 6,272,252 to Eldridge et al. ("Eldridge"), and U.S. Patent No. 5,739,868 to Butler et al. ("Butler").

In view of the amendments and remarks herein, Applicant respectfully traverses the rejections and asks that they be withdrawn. Applicant believes claims 1-23 to be in condition for allowance, and asks that all claims be allowed.

Claims 1, 8, 14, 18, and 22

Claim 1 is patentable over Kansal and Eldridge since neither reference teaches or suggests "setting an indicator in a line buffer," as recited in claim 1. For clarity, the claims have been amended to recite that the line buffer is "to store up to a full line of video overlay data."

The office action alleges that Eldridge discloses a line buffer. However, this is respectfully traversed. The cited portion (column 4, lines 20-31) does not teach using a line buffer. In fact, column 4, line 23-24 states that "The FIFO's must be a minimum of 16 scanlines of video data and rendering hints."

Further, the cited portion of Eldridge teaches an almost full indicator and an almost empty indicator, where the almost full indicator indicates when there is no longer room for one scanline in the FIFO, and where the almost empty indicator indicates when there is just one scanline in the FIFO. This teaching is not compatible with the idea of a line buffer. For a line buffer, the "almost full" indicator would trigger when the line buffer had any data at all (at which point there would no longer be room for one scanline in the line buffer), and the "almost empty" indicator would trigger when the line buffer was full (at which point there would be just one scanline in the line buffer).

Since neither Kansal nor Eldridge teach or suggest a line buffer as recited in claim 1, claim 1 is not obvious in view of Kansal or Eldridge, alone or in combination.

Further, there is no motivation in the references to modify Kansal to include a line buffer for video overlay data. The alleged motivation is that "Since Kansal and Eldridge are both systems with FIFO's with some type of indicator, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the line FIFO of Eldridge with the system of Kansal because FIFO only take lines of data." (See page 2 of the office action).

First, a FIFO may hold more or less than a line of data. For example, Eldridge teaches that its FIFO holds "a minimum of 16 scanlines of video data and rendering hints." (See column 4, lines 23-24 of Eldridge).

Second, the alleged motivation does not provide particular findings as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed," as required by the Federal Circuit in In re Sang Su Lee, 277 F.3d 1338, 1343 (Fed. Cir. 2002). Since these findings were not provided, it appears that the combination was made using impermissible hindsight.

Third, Applicant fails to see any motivation in the references for replacing the CRT FIFO of Kansal with a line buffer. The current inventors recognized that for video overlay data, providing a line buffer allows for completion of pixel processing (which includes, for example, horizontal and vertical zoom processing) in sufficient time to display consecutive overlay scan lines. In contrast, Kansal teaches a system for reading ahead display data into a display FIFO of a graphics controller. Applicant sees no motivation in the references to use a line buffer in such a system.

For at least this additional reason, claim 1 is patentable over Kansal and Eldridge, alone or in combination.

Claims 8, 14, 18, and 22 include similar features, and are therefore patentable for at least the same reasons as stated above with respect to claim 1.

Claims 2, 3, 10, 11, and 15

Claim 2 is patentable over Kansal and Eldridge because neither references teaches nor suggests "loading a first half of the data for the next video line when the pixel data being read reaches the indicator in the line buffer, and further comprises loading a second half of the data for the next video line when the pixel data being read reaches the end of the line buffer," as recited in claim 2. For support of this amendment please see, e.g., Figure 3 and page 7, line 19 to page 8, line 3 of the specification, and originally filed claim 11.

This feature provides the advantage that data for the next video line may be provided to the line buffer in two groups. First, when the pixel data being read reaches the indicator position in the buffer, the first half of the video data for the next video line may be loaded the line buffer. Second, when the pixel data being read reaches the end of the line buffer, the second half of the video data may be loaded.

Claims 3, 10, 11, and 15 include similar features, and are therefore patentable for at least this additional reason as well.

Claims 2-7, 9-13, 15-17, 19-21, and 23

Claims 2-7, 9-13, 15-17, 19-21, and 23 depend from claims 1, 8, 14, 18, and 22, and are therefore patentable for at least the same reasons as stated above with respect to independent claims 1, 8, 14, 18, and 22.